IN THE CLAIMS

Claim 1 (currently amended): A short-circuit detecting and protecting circuit comprising:

a switching unit for obtaining input signals,

a comparator including a first input terminal coupled to said switching unit, an output terminal, and a second input terminal, and including an internal voltage,

a load coupled to said first input terminal of said comparator,

a control transistor coupled between said switching unit and said second input terminal of said comparator, to ~~define input time of the input signals, and~~ detect the time when the input signals flowing to said comparator,

said switching unit including a first transistor coupled to said first input terminal of said comparator to obtain one of the input signals, and a second transistor coupled to said control transistor to obtain the other input signal,

means for detecting a voltage difference between said first and said second input terminal of said comparator, said detecting means including a detecting resistor coupled between said first and said second input terminals of said comparator, to generate and provide two voltage signals to said first and said second input terminals of said comparator respectively,

said comparator comparing the voltage difference between said first and said second input terminal of said comparator and internal voltage of said comparator, to determine a short-circuit or overload

situation.

Claim 2 (canceled).

Claim 3 (original): The short-circuit detecting and protecting circuit as claimed in claim 1, wherein said switching unit is a CMOS having a pMOS and an nMOS.

Claim 4 (canceled).

Claim 5 (original): The short-circuit detecting and protecting circuit as claimed in claim 1 further comprising a divider resistor coupled between said control transistor and said second input terminal of said comparator, to divide the signals.

Claim 6 (currently amended): The short-circuit detecting and protecting circuit as claimed in claim 1 ~~further comprising~~ wherein said load includes a load resistor coupled to said first input terminal of said comparator and ground.

Claim 7 (currently amended): A short-circuit detecting and protecting circuit comprising:

a switching unit including a first and a second switching transistors for obtaining first and second input signals respectively,

a first and a second control transistors coupled to said first and said second switching transistors of said switching unit respectively,

a first and a second comparators each including a first and a second input terminals and an output terminal, said first input terminal of said first comparator being coupled to said first control transistor via a first resistor, said second input terminal of said second comparator being coupled to said second control transistor via a second resistor, and

a load coupled between said second input terminal of said first comparator and said first input terminal of said second comparator, and

a first and a second detecting resistors coupled between said first input terminal of said first comparator and said second input terminal of said second comparator, to actuate either said first or said second comparator to output control signals.

Claim 8 (original): The short-circuit detecting and protecting circuit as claimed in claim 7, wherein said first switching transistor is a pMOS, and said second switching transistor is an nMOS.

Claim 9 (original): The short-circuit detecting and protecting circuit as claimed in claim 7 further comprising an overcurrent control means for switching off said short-circuit detecting and protecting circuit when receiving said output control signals from either said first or said second comparator.

Claim 10 (original): The short-circuit detecting and protecting circuit as claimed in claim 9, wherein said overcurrent control

means includes an OR gate coupled between said first and said second comparators.

Claim 11 (original): The short-circuit detecting and protecting circuit as claimed in claim 10, wherein said overcurrent control means further includes a first and a second control circuits coupled to said first and said second switching transistors of said switching unit respectively, and coupled to said OR gate.

Claims 12-14 (canceled).